MARCO FALTELLI

CONTACT INFORMATION

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RESEARCH INTERESTS

- High-Performance Computing, Fast Packet Processing, Hardware-Software Co-design, Parallel Computing, Data Center Networks, SmartNIC/FPGA offloading
- Network Drivers, Operative Systems

EDUCATION

University of Rome "Tor Vergata" PhD in Computer Science, Control and GeoInformation November 2019 - June 2023 Thesis: Towards resilient and effective network services Advisors: Prof. Giuseppe Bianchi, Prof. Francesco Quaglia Final Evaluation: Laude (top 5% quality)

October 2017 - October 2019 Master's Degree in Computer Engineering Thesis: A state-machine based platform for portable transport protocols Advisors: Prof. Giuseppe Bianchi, Prof. Francesco Quaglia Final Evaluation: 110/110 cum laude

Bachelor's Degree in Computer Engineering Final Evaluation: 110/110

TECHNICAL STRENGTHS

Programming Languages	C, C++, Java, Python, Javascript, Linux Kernel, Android, SQL, HTML
Programming Skills	non-blocking algorithms, code optimization, compilers, profilers, debuggers
HPC	MPI, OpenMP, RDMA, GPU offloading, HTCondor
Networking	SDN, NFV, DPDK, eBPF/XDP, Network Drivers, P4
Software & Tools	IDE, git, Matlab, R, MS Office, LaTeX
Frameworks & Services	Amazon AWS, ML (Tensorflow, Keras), Big Data (Hadoop, Flink)
Operative Systems	Linux, Windows 10, OS X

October 2014 - October 2017

Rome, Italy

WORK EXPERIENCE

ENEA	Frascati, Italy
Researcher	December 2023 - present
\cdot Researcher in the ICT-HPC department	
University of Rome "Tor Vergata"	Rome, Italy
Technologist	March 2023 - December 2023
 Parallel computing and code optimization methods for Quantum Computing - NextgenerationEU project 	the National Centre for HPC, Big Data and
Microsoft	Cambridge, United Kingdom
Research Intern	July 2022 - Oct. 2022
\cdot High-performing optimization methods for robots path planning in the Silica project	
NEC Laboratories Europe	Heidelberg, Germany
Research Intern	October 2021 - Dec. 2021

· Acceleration methods for 5G edge computing scenarios

October 2017 - December 2019 Student Researcher • Developer and maintainer for FlowBlaze and XTRA, open source projects for fast and stateful packet processing in hardware. Projects conducted under the H2020-5G PICTURE grant.

Rome, Italy

Rome, Italy

Nov. 2020 - March 2021

Worked on a railway use-case scenario for ensuring session continuity as part of the H2020-5G PICTURE project.

University of Rome Tor Vergata Computer Science tutor

AWARDS & HONORS

- · Winner of a 2022 Microsoft Research PhD Fellowship
- · Partecipation to the 2023 CERN School of Computing

• "A Fully Portable TCP Implementation Using XFSMs" has earned the 3rd place in the ACM SIG-COMM 2018 Student Research Competition (Undergraduate class).

· Winner of a scholarship from the Italian Ministry of Education for outstanding student results in 2017.

PUBLICATIONS

- M. Faltelli, G. Belocchi, F. Quaglia, S. Pontarelli, and G. Bianchi. Metronome: adaptive and precise intermittent packet retrieval in DPDK (extended version). In IEEE/ACM Transactions on Networking, Oct. 2022
- M. Faltelli, G. Belocchi, F. Quaglia, S. Pontarelli, and G. Bianchi. Metronome: adaptive and precise intermittent packet retrieval in DPDK. In ACM CoNEXT 2020
- G. Bianchi, M. Welzl, A. Tulumello, F. Gringoli, G. Belocchi, M. Faltelli, and S. Pontarelli. XTRA: Towards Portable Transport Layer Functions. IEEE Transactions on Network and Service Management, Dec 2019

CNIT

- V. Bruschi, M. Faltelli, A. Tulumello, S. Pontarelli, F. Quaglia, and G. Bianchi. Offloading online MapReduce tasks with stateful programmable data planes. In *IEEE NETPROC 2020*
- G. Bianchi, M. Faltelli, and V. Bruschi. Back to the Future: Towards Hardware "Netputing" Architectures. In *IEEE MedComNet 2020*
- G. Bianchi, M. Welzl, A. Tulumello, G. Belocchi, M. Faltelli, and S. Pontarelli. A Fully Portable TCP Implementation Using XFSMs. In ACM SIGCOMM 2018 Posters and Demos
- M. Spaziani Brunella and M. Faltelli. Exploiting Foreshadow-VMM. Technical report, CNIT, 2019